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JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,101	FILIPPO ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8 Stepmber 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending.

Papers Filed

2. Examiner acknowledges receipt of RCE filed 08 September 2006.

New Rejections

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Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 12 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb in view of common art and Hughes in view of common art and Hughes in view of common art.

Regarding claims 12 and 30, Hughes and Web disclose the microprocessor of claim 9 and the method of claim 28.

It is believed by Examiner to be inherent that a program must reissue at least some element of the previous instruction to receive a desired output; however this is not expressed explicitly in either reference.

Examiner asserts it is common in the art to reissue instructions when the output is not a desired result.

Hughes and Web would have been motivated to utilize this technique because reissuing instructions is a common, simple, fast, and effective technique for gaining the correct output. In fact, Examiner is not aware of any other technique.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of either Hughes and Web and combine it with the ability to reissue instructions when the original output is not a desired result.

Maintained Rejections

2. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-6, 8-22, 24-25 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (International Application WO 01/35212) which was cited on Applicant's information disclosure statement filed 27 February 2006.

5. As per claims 1 and 14, Hughes discloses a microprocessor and computer system, comprising: a dispatch unit configured to dispatch load and store operations (page 12 lines 6-12); and a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit (Fig. 1), wherein the load store unit includes an indexed STLF (Store-to-Load Forwarding) buffer (Fig. 1), wherein the indexed STLF buffer includes a plurality of entries (Fig. 1 and page 15 lines 24-28); wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to index into the indexed STLF buffer using the general index to select one of the plurality of entries, and to forward data included in the one of the plurality of entries as a result of the load operation. (page 34 lines 21-30 and claims 1-2)

6. As per claims 2 and 15, Hughes discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation. (page 34 lines 21-30 and claims 1-2) *The examiner asserts that if the address does not match, an entry is not forwarded on a data load operation.*

7. As per claims 3 and 22, Hughes discloses the microprocessor of claim 1 and the method of claim 20, wherein the one of the plurality of entries in the STLF buffer is configured to store an address, data, and a data size (Fig. 1) associated with a store operation.

8. As per claims 5, 16 and 24, Hughes discloses the microprocessor of claim 1, computer system of claim 14 and the method of claim 20, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation. (Fig 1 ADDR - Tag)

9. As per claims 6, 17 and 25, Hughes discloses the microprocessor of claim 5, computer system of claim 14 and the method of claim 24, wherein the load store unit is configured to generate the additional index dependent on both the at least the portion of the address of the store operation and a number of bytes of data operated on by the store operation, and wherein the load store unit is configured to generate the index dependent on both the at least a portion of the address of the load operation and a number of bytes of data operated on by the load operation. (Page 8 lines 10-13) *The examiner asserts that the data size is used as an index to determine if a TRAP signal is to be generated due to a load requesting a larger block of data than was previously stored at that memory location.*

10. As per claims 8 and 27, Hughes discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Fig 1 ADDR - Tag)

11. As per claims 9 and 18, Hughes discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. (Fig. 1 Hit control Circuit 402 and page 2 lines 28-32)

12. As per claims 10 and 28, Hughes discloses the microprocessor of claim 9 and the method of claim 20, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation. (Page 8 lines 14-17)

13. As per claims 11, 19 and 29, Hughes discloses the microprocessor of claim 9, computer system of claim 14 and the method of claim 28, wherein the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer. (Page 5 lines 15-18)

14. As per claims 12 and 30, Hughes discloses the microprocessor of claim 9 and the method of claim 28, wherein the STLF checker is configured to replay one or more additional operations that are dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer. (Page 5 lines 15-18) *The examiner asserts that after an initial load instruction is attempted and fails, any other instructions which have been issued which depend on the load instruction for data must be replayed once the data has been made available through the replay of the load operation.*

15. As per claims 13 and 31, Hughes teaches the microprocessor of claim 9, wherein the load store unit is configured to identify the result of the load operation as a speculative value in response to forwarding the data in the one of the plurality of entries included in the STLF buffer as the result of the load operation; wherein if the STLF checker verifies that the STLF buffer operated correctly for the load operation, the load store unit is configured to indicate that the result of the load operation is not speculative. (abstract and claims 1-4)

16. As per claim 20, Hughes discloses a method, comprising: receiving an address of a load operation; generating an index corresponding to the address; using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding) buffer; and forwarding data included the entry as a result of the load operation. (abstract, Fig. 1 and page 15 lines 24-28)

17. As per claim 21, Hughes discloses the method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation. *The examiner asserts that the forwarding of an entry is dependant on the physical address matching.*

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes.

20. As per claims 4 and 23, Hughes discloses the microprocessor of claim 1 and the method of claim 20, but fails to disclose each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation. Hughes does not disclose the data bus width of the processor of his invention.

21. Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely well known in the art. With any of these data buses in place in Hughes' invention, the data buffer would be able to hold at least the maximum amount of data specified by a data store operation.

22. A data bus having a given size less than or equal to 64 bits is beneficial in a processor in that costs of implementation are limited. Larger data buses require processor components to also grow in size, increasing processor area, power consumption and cost.

23. Implementing a data bus less than or equal to 64 bits in Hughes' invention would have been obvious at the time of invention to one of ordinary skill in the art for the benefit of limiting costs, size and power consumption.

24. Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes in view of Hennessy (Hennessy, J. L., Patterson, D. A. Computer Organization and Design. Morgan Kaufmann Publishers, Inc.: 1998. Pages 549-550.)

25. As per claims 7 and 26, Hughes discloses the microprocessor of claim 6 and the method of claim 25, but fails to disclose that the additional index is generated by right-shifting a lower portion of the address targeted by the store operation by an amount equal to a logarithm in base two of the number of bytes of data operated on by the store operation.

26. Hennessy discloses indexing a cache by means of the lower portion of an address, minus the appropriate offset for minimum memory access size (byte, in Hennessy's case) (Fig. 7.7 and page 549-550) Right shifting is an extremely well-known method of eliminating undesired bits to the right of desired bits.

27. Hennessy teaches that removing the two bits for the byte offset reduces the total cache size, as fewer bits must be kept in the tag field of each entry. A smaller cache size takes up less space on chip and is less expensive to implement.

28. It would have been obvious to one of ordinary skill in the art at the time of invention to have included the method of generating a cache index disclosed by Hennessy in Hughes' invention for the benefit of reducing necessary cache size.

Previously Maintained Rejections

29. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 102

30. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

31. Claims 1-3, 5-6, 8-12, 14-22, 24-25 and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Webb et al. (U.S. Patent No. 6,360,314) hereinafter referred to as Webb.

32. As per claims 1 and 14, Webb discloses a microprocessor and computer system, comprising: a dispatch unit configured to dispatch load and store operations (Fi.g 1 clock cycle: Issue) *The examiner asserts that a unit is responsible for issuing operations*; and a load store unit configured to store information associated with load and store operations dispatched by the dispatch unit (Fig. 4), wherein the load store unit includes an indexed STLF (Store-to-Load Forwarding) buffer (Fig. 4 buffer 428 and queue 426), wherein the indexed STLF buffer includes a plurality of entries (Fig. 7); wherein the load store unit is configured to generate an index dependent on at least a portion of an address of a load operation, to index into the indexed STLF buffer using the general index to select one of the plurality of entries (Col. 5 lines 5-8 and 19-22), and to forward data included in the one of the plurality of entries as a result of the load operation. (Col. 2 lines 8-15)

33. As per claims 2 and 15, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit is configured to not forward the data included in the one of the plurality of entries as the result of the load operation if information included in the one of the plurality of entries does not match information associated with the load operation. (Col. 2 lines 7-15) *The examiner asserts that if the address does not match, an entry is not forwarded on a data load operation.*

34. As per claims 3 and 22, Webb discloses the microprocessor of claim 1 and the method of claim 20, wherein the one of the plurality of entries in the STLF buffer (Fig. 7) is configured to store an address (Fig. 7 address 42), data (Fig. 7 word 52), and a data size (Fig. 7 size 48) associated with a store operation.

35. As per claims 5, 16 and 24, Webb discloses the microprocessor of claim 1, computer system of claim 14 and the method of claim 20, wherein the load store unit is configured to select which one of the plurality of entries to allocate to a store operation by generating an additional index dependent on at least a portion of an address of the store operation. (Col. 5 lines 5-8 and 19-23)

36. As per claims 6, 17 and 25, Webb discloses the microprocessor of claim 5, computer system of claim 14 and the method of claim 24, wherein the load store unit is configured to generate the additional index dependent on both the at least the portion of

the address of the store operation (Col. 5 lines 5-8 and 19-23) and a number of bytes of data operated on by the store operation (Col. 6 lines 51-59), and wherein the load store unit is configured to generate the index dependent on both the at least a portion of the address of the load operation and a number of bytes of data operated on by the load operation. *The examiner asserts that the data size is used as an index to determine if a TRAP signal is to be generated due to a load requesting a larger block of data than was previously stored at that memory location.*

37. As per claims 8 and 27, Webb discloses the microprocessor of claim 5 and the method of claim 24, wherein the additional index comprises a portion of the address targeted by the store operation. (Col. 5 lines 19-22)

38. As per claims 9 and 18, Webb discloses the microprocessor of claim 1 and computer system of claim 14, wherein the load store unit further comprises a STLF checker configured to verify operation of the STLF buffer. *The examiner asserts that Webb's invention contains a unit which verifies operation, specified as the apparatus disclosed in col. 7, lines 5-8.*

39. As per claims 10 and 28, Webb discloses the microprocessor of claim 9 and the method of claim 20, wherein the STLF checker is configured to perform an associative address comparison to identify all issued store operations targeting a same address as

the load operation and to implement a find-first algorithm to select a youngest issued store operation that is older than the load operation. (Col. 7 lines 3-36)

40. As per claims 11, 19 and 29, Webb discloses the microprocessor of claim 9, computer system of claim 14 and the method of claim 28, wherein the STLF checker is configured to replay the load operation if the STLF checker identifies incorrect operation of the STLF buffer. (Col. 1 lines 34-38) *The examiner asserts that if a load operation does not result in data being provided from the cache, the memory load is replayed to main memory.*

41. As per claims 12 and 30, Webb discloses the microprocessor of claim 9 and the method of claim 28, wherein the STLF checker is configured to replay one or more additional operations that are dependent on the load operation if the STLF checker detects incorrect operation of the STLF buffer. (Col. 7 lines 63-65) *The examiner asserts that after the inflight instructions are killed, they must inherently be reissued. If the instructions are not reissued, the program may produce undesired output or simply cease operation.*

42. As per claim 20, Webb discloses a method, comprising: receiving an address of a load operation; generating an index corresponding to the address; using the index to select an entry from a plurality of entries included in a STLF (Store-to-Load Forwarding)

buffer; and forwarding data included the entry as a result of the load operation. (Col. 5 lines 5-22)

43. As per claim 21, Webb discloses the method of claim 20, wherein said forwarding is dependent on information included in the entry matching information associated with the load operation. *The examiner asserts that the forwarding of an entry is dependant on the physical address matching.*

Claim Rejections - 35 USC § 103

44. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. Claims 4 and 23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb.

46. As per claims 4 and 23, Webb discloses the microprocessor of claim 1 and the method of claim 20, but fails to disclose each of the plurality of entries in the STLF buffer has a capacity to store a maximum amount of data that can be written by a store operation. Webb further discloses the data entry to hold any of a quadword, longword, word or byte (Col. 4 line 66-67) but does not disclose the data bus width of the processor of his invention.

47. Official Notice is taken that data buses of sizes 8, 16, 32 or 64-bit are extremely well known in the art. With any of these data buses in place in Webb's invention, the data buffer would be able to hold at least the maximum amount of data specified by a data store operation.

48. A data bus having a given size less than or equal to 64 bits is beneficial in a processor in that costs of implementation are limited. Larger data buses require processor components to also grow in size, increasing processor area, power consumption and cost.

49. Implementing a data bus less than or equal to 64 bits in Webb's invention would have been obvious at the time of invention to one of ordinary skill in the art for the benefit of limiting costs, size and power consumption.

50. Claims 7 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb in view of Hennessy (Hennessy, J. L., Patterson, D. A. Computer Organization and Design. Morgan Kaufmann Publishers, Inc.: 1998. Pages 549-550.)

51. As per claims 7 and 26, Webb discloses the microprocessor of claim 6 and the method of claim 25, but fails to disclose that the additional index is generated by right-shifting a lower portion of the address targeted by the store operation by an amount equal to a logarithm in base two of the number of bytes of data operated on by the store operation.

52. Hennessy discloses indexing a cache by means of the lower portion of an address, minus the appropriate offset for minimum memory access size (byte, in Hennessy's case) (Fig. 7.7 and page 549-550) Right shifting is an extremely well-known method of eliminating undesired bits to the right of desired bits.

53. Hennessy teaches that removing the two bits for the byte offset reduces the total cache size, as fewer bits must be kept in the tag field of each entry. A smaller cache size takes up less space on chip and is less expensive to implement.

54. It would have been obvious to one of ordinary skill in the art at the time of invention to have included the method of generating a cache index disclosed by Hennessy in Webb's invention for the benefit of reducing necessary cache size.

Response to Arguments

1. Applicant's arguments filed 8 September 2006 have been fully considered but they are not persuasive.

2. Several of Applicant's arguments question whether using a value (whether it be data size or a portion of an address or a combination) can be considered "indexing". Foldoc.org, an online computing dictionary, uses the following definition, "a number used to select an element of a list, vector, array or other sequence". The bits used as an index constitute a number; the entries of the STL buffer are considered to be elements of a list; and both prior art references select based on the requirements of the definition. Additionally, there are several arguments with regard to "generating an index". An index, as interpreted in this Office Action, can be generated in at least two ways: 1) When the bits used for the index are determined based on the output of any logic components or 2) taking the pre-existing bits and organizing them in a fashion that they can be utilized as an index.

Regarding Hughes,

3. Applicant states:

"Regarding claim 5...Hughes...[teaches that] '[t]he address tag portion is the portion of the address which is stored as a tag by the data cache...' Thus, this tag is clearly not generated by the load store unit and used in selecting an entry in the STLF buffer, as required by Applicants' claim 5."

Examiner disagrees. The tag is considered to be generated by the load/store unit because it assists in load/store processes. Typically, claiming that an element is creating "by another element" is given little patentable weight. Calling a particular portion of a processor a "load/store unit" is simply a conceptual viewpoint for understanding the processor. A real processing system contains logic placed anywhere that will limit space, energy and timing requirements. Within the actual invention,

particular "units" have no real meaning outside of a conceptual analysis. Consequently, it is reasonable for Examiner to interpret whatever element "generates" a tag to be part of the load/store unit. Additionally, the tag is used in selecting an entry from the STLF buffer. See Hughes page 7 lines 10-14.

4. Applicant states:

"Regarding claim 10...Hughes...[makes] no mention of implementing a find-first algorithm"

Examiner disagrees. It is unclear what definition Applicant believes the claimed invention requires from the term "find-fast algorithm", but it appears sufficient to say that the remainder of the functionality of claim 10 can be considered a "find-fast algorithm" and Applicant says nothing to suspect the contrary.

5. Applicant states:

"Regarding claim 11, [there is] no mention of an instruction or operating being replayed anywhere in Hughes....Furthermore, the response does not include replaying the load operating, but may include filling the data cache with a cache line read by the load or with fill data, which may result in a cache hit if the load is reattempted."

Examiner disagrees. The "replay" is being interpreted broadly as stated in an Office Action mailed 02 June 2006 and below with respect to Webb. Additionally, the fact that a reattempted load "may result" in a cache hit does not prevent the remaining times that this is not the case from anticipating the claim.

6. Applicant states:

"Regarding claim 12,...The Examiner asserts, '...after an initial load instruction is attempts and fails, any other instructions which have been issued which depend on the load instruction for data must

be replayed once the data bas been made available through replay of the load operation.' This is purely speculation by the Examiner."

See the response with regard to Webb below. Additionally, an Official Notice rejection has been added in attempt to address Applicant's concern.

7. Applicant states:

"Regarding claim 13,...[n]one of the limitations of claims 1-4 has anything to do with identifying a result of a load operation as speculative or with indicating that the result of the load operation is not speculative if the STLF checker verifies correct operation of the STLF buffer for the load operation."

See Abstract lines 14-20.

8. Applicant states:

"Applicants assert that the Examiner's Official Notice does not teach or suggest the limitations of claim 4."

See arguments below with respect to Webb. Also see below with regard to the arguments of claim 7.

Regarding Webb,

9. Applicant states:

"FIG. 4 clearly illustrates that store data buffer 428 and store queues 426 are components of data cache subsystem 420, and not load/store unit 418.

The following is a quote from an office action mailed 02 June 2006:

"The examiner further notes that the STLF buffer and associated logic constitute part of the load/store unit as they all assist in performing load and store operations."

10. Applicant states:

"Further regarding claim 1...there is nothing in these citations that teach that the load store unit, or any other apparatus, is configured to generate an index."

It is unclear to Examiner how Applicant believes the index came into existence without being "generated".

11. Applicant states:

"Furthermore, the index referred to in these citations is not a generated index used to index into an indexed STLF buffer, or to Webb's store queue 426 and store data buffer 428, which the Examiner equates with Applicants' STLF buffer. Instead, these citations describe indexing into dcache unit 430, and its components."

Examiner disagrees. The bits described in col 5 lines 19-22 are used to index the STL buffer as well (col 6 lines 6-10).

12. Applicant states:

"Regarding claim 5,...there is nothing in Webb that teaches the load store unit is configured to generate...two indices"

Examiner disagrees. The "additional index" as claimed is required to depend on a portion of the address of the store operation (col. 5 liens 5-8 and 19-23) and data operated on by the store operation (col. 6 liens 51-59). Examiner asserts that the combination of this data is considered to be an "additional index".

Applicant states:

"Regarding claim 6,...using a comparison of two data size values to generate a signal is clearly not the same as generating an index dependant on a data size value."

Examiner disagrees. The indexes are matched against every entry in the store queue. The fact that a signal is generated in response to this indexing is immaterial.

13. Applicant states:

"Regarding claim 9...column 7, lines 5-8...does not describe a unit configured to verify operation of the STLF buffer, as recited in claim 9, but describes only one of the operations of 'a methodology and apparatus' for choosing which of the multiple stores should be used."

Examiner disagrees. This determination is considered to be verifying the operation of the STLF buffer. Examiner believes this is a fair and reasonable interpretation. The fact that the citation only describes "one of the operations" does not prevent it from anticipating the clause of claim 9. The claim does not specify that all operation is verified.

14. Applicant states:

"Regarding claim 9...Examiner submits, 'there must inherently exist logic to verify that the correct entry is forwarded when multiple stores are pending for the same address'...Applicants remind the Examiner that 'to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the things described in the reference'...Inherency, however, may not be established by probabilities or possibilities"

Examiner asserts that the use of inherency is correct in this claim. The functionality considered to be inherent is required for proper functionality of the invention as disclosed. If incorrect entries were forwarded, the processor would be broken and unable to function as the reference states. There is no use of "probabilities" or "possibilities". Applicant also suggests that there is no "checker configured to verify". Examiner reiterates that there must be logic to insure the proper verification. Perhaps Applicant believes that the word "verify" requires some redundant checking of a

processor's functionality. If so, Examiner disagrees. Correct functionality is all that is required by the claims to satisfy this verification.

15. Applicant states:

"Regarding claim 11...Examiner submits, '...There is nothing in applicant's specification defining the term 'replay' and hence, it has been awarded its broadest reasonable definition.'...Applicant's disagree with...[Examiner's] assertion that Applicants' specification does not include anything defining this term."

Applicant's contention that the portion of the specification provided is a suitable definition is incorrect. The specification says "e.g., by providing a signal to the scheduler 118". This is referring to an example of how the word replay must be used, not a particular definition for the word. Without a suitable definition, it is improper for Examiner to read limitations from the specification into the claims.

16. Applicant states:

"Regarding claim 12...Applicants assert that the system of Webb could respond to the TRAP signal in any number of ways to produce the correct output or prevent the program from ceasing operation"

Examiner disagrees. If a program has an undesired output, it must reissue at least some element of the previous instruction to receive a desired output. Examiner maintains the contention that this is inherent. Applicant believes that there are several other options available, in which case Applicant is invited to suggest other possibilities. This appears to be an inherent aspect of the invention.

However, in effort to alleviate Applicant's concern on this issue, Official Notice has been taken with regard to claim 12.

17. Regarding claims 13 and 31 in view of Webb, it appears that this rejection has been withdrawn in the most recent action. Consequently, this argument is moot.

18. Applicant states:

"Regarding claim 4...[a]pplicant's assert that the maximum amount of data that can be written by a store operation is not necessarily the same as, or dependent on, the data bus width."

Examiner asserts that the claim language calls for "a capacity" which is defined as "the ability to receive or contain" by the American Heritage Dictionary. Examiner further asserts that the appropriately sized data bus is an ability to receive.

19. Applicant states:

"Regarding claim 7...[a]pplicants assert...that claim 7 has nothing to do with indexing a cache or reducing a cache size...Webb does not teach generating this additional index, so one would not have any reason to explore ways to generate such an index."

Examiner disagrees. The additional index is generated in Webb, as previously discussed. Consequently, an obvious rejection with an analogous and extremely common technique is reasonable in this case.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.